Change Approved 6/1/05 PJ

IN THE SPECIFICATION:

The specification as amended below with replacement paragraphs shows added text with underlining and deleted text with ~~strikethrough~~.

Please REPLACE the paragraph beginning at page 31, line 24, with the following paragraph:

Fig. 23 is a block diagram showing in detail another structure of the pattern generating part in the testing apparatus according to the first embodiment of this invention. The pattern modifier 4 shown in Fig. 423 comprises, instead of the multiplexers 23 shown in Fig. 4, OR (logical sum) circuits 28, AND (logical product) circuits 29, and F/Fs 30 each holding the inverted state independently of the lead F/F on the scan path. The overhead of the circuit is increased a little because the structure as shown in Fig. 23 is employed as a structure of the pattern modifier 4, but it becomes easy to completely separate the LFSR (pattern generator) 2 from the scan paths #0 to #127 to modularize them, and a reordering process of optimizing the order of the scan F/Fs at the time of layout for physical placement and routing becomes possible.

Please change this "Fig. 23" to, PJ. 6/1/05.